EE/CprE/SE 492 BIWEEKLY REPORT 1

Date: ***August 21st, 2023 – September 16th***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

Biweekly Summary

For the start of this second semester of senior design, we got back into the swing of things and started back up on our progress from the previous semester. Over the summer, NGSpice adopted OSDI (open-source device interface), which allows Verilog-A models to be run in Spice. This is major for us because the device model for the ReRAM device in the Skywater 130 nm process is written in Verilog-A, while all other components were written in Spice. Before, we were worried about how we were going to simulate all of our components together since they were not all one standard. However, now, with NGSpice adopting this OSDI support, it becomes much easier to simulate everything under one spice simulation with the OSDI support on, so the Verilog-A can be read in.

So, we worked on getting an updated version of NGSpice with the OSDI support enabled. Once we did that, we went and simulated the ReRAM device under a spice simulation and compared the results with the results we got from Xyce to ensure everything was as expected. The waveforms matched, so we feel confident that we can use NGSpcie with OSDI compatibility for all simulations for our devices now.

More progress was made on pushing some of our devices through the analog process flow. This step is still slow going as we are having trouble getting the expected post-layout results from our 1-bit ADC. However, we were able to make some improvements in the post-layout simulation results by changing the layout of the 1-bit ADC slightly according to some

videos that were posted by Efabless over the summer. We also asked in the Slack channel what could be the issue, as somebody in there may be able to better identify what the issue is. We also made more progress on our 3-bit ADC by getting a schematic created for it and getting acceptable simulation results.

Finally, we updated the digital model of the ReRAM device (this model just shows the expected behavior of the ReRAM crossbar with our current understanding) according to some things we learned at the end of last semester. We also worked on getting the analog framework provided by Efabless to work correctly, but this still appears to be broken from last semester. We have contacted Efabless to let them know of this issue, and we will see if they are able to correct it on their end.

Past Weeks Accomplishments

- Joshua Thater
    - Reconfigured NGSpice with the OSDI enabled support
    - Obtained an updated model of the ReRAM device that was able to be simulated with the new OSDI support
        - Simulated the new ReRAM device with a Spice simulation and got the same results as from the Xyce simulations - very good news as this will alleviate many headaches with having to jump between Verilog-A and Spice models
    - Worked on getting analog simulations of 1T1R cell
        - Created schematic and testbench for this cell
        - Got a better understanding of how the form and write/read operations are supposed to work with the ReRAM device thanks to the table laid out in the documentation for the device: https://sky130-fd-pr-reram.readthedocs.io/en/latest/technology_specifications.html#forming
    - Worked on getting the correct layout of ReRAM cell
- Aiden Petersen
    - Updated digital behavior model
        - Changed LA pins
        - More accurately models analog implementation
        - Does a MAC instead of a matrix multiplication
    - Attempted to setup analog design framework again and failed
- Matt Ottersen
    - Worked on layout for Op Amp
        - Did a redesign of the layout that had better overall performance, but still does not meet our expectations as its gain is very low
- Regassa Dukele

- Able to integrate my design into a new VM
- Designed 3-bit ADCs
- Created a test bench for ADC and did a simulation

Pending Issues

- How to actually perform the write/read operations with analog simulations - is it even possible with the simplified model we are given?
- Creating a layout of ReRAM device that passes both DRC and LVS checks
- Digital behavioral model bugs exist
- Analog design framework doesn't work
- Drivers out of date
- Components, when instantiated in layout, are not performing as expected

Individual Contributions

Team Member	Individual Contributions	BIweekly Hours	Total Hours
Joshua Thater	Reconfigured NGSpice with OSDI and got Spice simulations of the ReRAM device. Continued work on getting 1T1R simulations	17	80
Aiden Petersen	Debugging analog design framework. Updated digital behavioral design.	12	68
Matt Ottersen	Worked on Op Amp Layout	12	68
Regassa Dukele	Designed ADCs, developed a test bench for ADC, and conducted a simulation.	15	72

Plans for the Upcoming Weeks

- Joshua Thater
    - Ask questions in the Slack channel to get clarity and help with many aspects of our project.
        - Can we actually perform write/read operations of the 1T1R cell with the device model we are given? How?
        - How can we verify that a write was actually successful?
        - How to correctly set up testbenches to observe the expected behavior?
    - Create a brief write–up on how to get analog design flow set up to help senior design team that is starting up this semester
        - Will probably also do a write-up on how to get ReRAM simulation set up with NGSpice as well

    - Continue to work on getting the ReRAM layout to pass DRC and LVS checks - will probably need to ask clarifying questions in the Slack channel
- Aiden Petersen
    - Fix analog design framework
        - Ask questions on the slack
    - Update drivers and document LA communication
    - Fix digital behavioral design bugs
- Matt Ottersen
    - Continue working on Op Amp and ADC Layout
        - Ask questions about it on Slack
        - Troubleshoot component performance in layout compared to schematic
- Regassa Dukele
    - Working on addressing some design issues and making necessary corrections.
        - Posted a question on Slack regarding some design issues
        - Make necessary changes
    - Make layout for OpAmp and ADC.